Claims

1. A low drop-out voltage regulator comprising:

transistor means (Q1-Q2) for receiving a reference voltage and in dependence thereon producing a regulated output voltage;

an output stage (Q3) for coupling to a load;

first direct current (DC) control loop means (310) coupled to the transistor means (Q1-Q2) for providing a dominant pole; and

second direct current (DC) control loop means (320) for providing a non-dominant pole, whereby stability of operation may be obtained with a lower load capacitance.

2. The low drop-out voltage regulator as claimed in claim 1 wherein the control loop means (310) comprises:

differential amplifier means (B) having an output coupled to the transistor means (Q1, Q2); and

voltage divider means (r_1, r_2) coupled between the voltage regulator output and a first input of the differential amplifier means.

3. The low drop-out voltage regulator as claimed in claim 2 wherein the control loop means (310) further comprises:

voltage reference means coupled between the voltage regulator output and a first input of the differential amplifier means.

4. The low drop-out voltage regulator as claimed in claim 1, 2 or 3 wherein the output stage (Q3) comprises a low impedance output.

5. A low drop-out voltage regulator as claimed in any preceding claim wherein the second direct current (DC) control loop means (320) is coupled to the voltage regulator output and first direct current (DC) control loop means.

6. A low drop-out voltage regulator as claimed in any preceding claim wherein the second direct current (DC) control loop means (320) has a unity direct current (DC) gain.

7. The low drop-out voltage regulator as claimed in any preceding claim wherein the transistor means (Q1-Q2) comprises a cascode transistor arrangement.

8. The low drop-out voltage regulator as claimed in any preceding claim wherein the output stage comprises a cascode transistor arrangement.

9. The low drop-out voltage regulator as claimed in any preceding claim wherein the output stage comprises a P-type transistor.

10. The low drop-out voltage regulator as claimed in claim 9 wherein the P-type transistor is a PMOS transistor.

11. The low drop-out voltage regulator as claimed in any preceding claim wherein the transistor means (Q1-Q2) comprises at least part of the second direct current (DC) control loop means (320).

12. A method for low drop-out voltage regulation comprising:

providing transistor means (Q1-Q2) receiving a reference voltage and in dependence thereon producing a regulated output voltage;

providing an output stage (Q3) for coupled to a load;

providing first direct current (DC) control loop means (310) coupled to the transistor means (Q1-Q2) for providing a dominant pole; and

second direct current (DC) control loop means (320) and providing a non-dominant pole, whereby stability of operation may be obtained with a lower load capacitance.

13. The method for low drop-out voltage regulation as claimed in claim 12 wherein the control loop means (310) comprises:

differential amplifier means (B) having an output coupled to the transistor means (Q1, Q2); and

voltage divider means (r_1, r_2) coupled between the voltage regulator output and a first input of the differential amplifier means.

14. The method for low drop-out voltage regulation as claimed in claim 13 wherein the control loop means (310) further comprises:

voltage reference means coupled between the voltage regulator output and a first input of the differential amplifier means.

15. The method for low drop-out voltage regulation as claimed in claim 12, 13 or 14 wherein the output stage (Q3) comprises a low impedance output.

16. The method for low drop-out voltage regulation as claimed in any one of claims 12-15 wherein the second direct current (DC) control loop means (320) is coupled to the voltage regulator output and first direct current (DC) control loop means.

17. The method for low drop-out voltage regulation as claimed in any one of claims 12-16 wherein the second direct current (DC) control loop means (320) has a unity direct current (DC) gain.

18. The method for low drop-out voltage regulation as claimed in any one of claims 12-17 wherein the transistor means (Q1-Q2) comprises a cascode transistor arrangement.

19. The method for low drop-out voltage regulation as claimed in any one of claims 12-18 wherein the output stage comprises a cascode transistor arrangement.

20. The method for low drop-out voltage regulation as claimed in any one of claims 12-19 wherein the output stage comprises a P-type transistor.

21. The method for low drop-out voltage regulation as claimed in claim 20 wherein the P-type transistor is a PMOS transistor.

22. The method for low drop-out voltage regulation as claimed in any one of claims 12-21 wherein the transistor means (Q1-Q2) comprises at least part of the second direct current (DC) control loop means (320).

23. An integrated circuit comprising the low drop-out voltage regulator of any one of claims 1-11.